Remarks

Formal acceptance and consideration therefor of this amendment which, applicants submit, renders the application allowable, is respectfully requested. Supportive discussion/rebuttal arguments directed thereto follows.

The earlier submitted Substitute Specification was further revised to remove additionally noted informalities. The revisions/corrections being made to the Substitute Specification are also inclusive of the listed informalities on page 2 of the outstanding Office Action. Acceptance and formal entry of the same is respectfully requested.

Applicants note, with appreciation, also, the allowance of claims 8-27 and 30-32. With the above made amendments, claims 1-32, 34-35 and 51-56 remain pending of which claims 1, 4 and 34 are currently amended and claims 51-56 are newly presented. Incidentally, original claims 36-50 have been canceled strictly to avoid an additional claim fee with the submission of the new claims 51-56. The canceling of the previously withdrawn claims was made without prejudice or disclaimer of the subject matter, in which also applicants reserve their right to subsequently file a divisional application directed thereto. By this amendment, claim 33 was also canceled.

Claim 34 was revised to clarify the last subparagraph therein. This portion now clearly sets forth that the second semiconductor regions which are formed through an impurity diffusion from the conductive film serve as the source and drain regions (of a field effect transistor). An example of this is seen with regard to the disclosed third embodiment in the Specification such as it relates to Figs. 42-47 of the drawings, although not limited thereto. For example, n-type regions 15a, 15b on

either side of the buried gate structure such as shown in Fig. 46, although not limited thereto, relate to the source and drain regions. In this example, after the formation of the plug 47 within the contact hole 45, similarly as done on the plug 22 side (or bit line side) of the memory cell selection MISFET, there is effected diffusion of impurities from the plug 47 into the semiconductor substrate 1 such that an upper high concentration region 15b, associated with the source/drain region, is formed (see the related discussion in paragraph [0166] on page 50 of the Substitute Specification). With regard to the disclosed example first embodiment, see a similarly related discussion in paragraph [0141], on page 36 of the Substitute Specification, and Fig. 27 of the drawings. In this example, phosphorus ions are diffused into the substrate 1 from the plug 22 such that high concentration regions are formed in the p well for the sources and drains of MISFETs having a buried gate structure.

Regarding the set forth "first insulating film" and the "second insulating film," according to claims 28-29 and 34-35, an example of these are shown by the example third embodiment of the present application, although not limited thereto, in which CAP insulating film 42a, which is made of silicon nitride material, relates to the "first insulating film" and silicon oxide film 20 relates to the "second insulating film." Related discussion of this is found in connection with Figs. 40-43. Because the CAP layers 42a are formed of silicon nitride material and the upper insulating layer 20 is formed of silicon oxide material by a CVD method, characteristic differences in the etching rates occur. As a result, the contact holes 21 can be prevented from reaching the gate electrodes 9 because of the effective slow etching rate of the CAP insulating film 42a even in the case where over-etching may occur at the time of forming the contact holes 21. Related discussion insofar as applicable

to the example 3 embodiment, although not limited thereto, is given in paragraph [0162] on page 49 of the Substitute Specification.

It is submitted, in view of the clarifying revisions to independent claim 34 as well as the above supportive discussion directed thereto including with regard to the claimed first and second insulating films, the presently outstanding rejection under 35 USC §112, second paragraph, is accordingly traversed and reconsideration and withdrawal thereof is respectfully requested.

In view of the supportive discussion contained hereinabove regarding claim 28 (dependent on allowable claim 27) and claim 29 (dependent on claim 28), favorable action therefor is also requested with regard to these claims.

Regarding base claim 1, amendments were made thereto in consideration of effecting further clarification of the invention claimed including in connection with further highlighting the improved featured aspects of the buried gate technique of the field effect transistors (of the memory cells) set forth therein and in a manner which highlights various distinguishing aspects thereof over the art, as applied in the rejection. Similar such revisions were also implemented in independent claim 4. Newly presented claims 51-56 were added in consideration of more fully covering the various featured aspects directed to the method of manufacture of a semiconductor integrated circuit as that originally set forth. As in claims 1+, 4+, as well as in allowed claims 8+, 10+, 17+ and, also in claims 34+, the invention according to claims 51-56 sets forth a buried gate structure scheme in connection with the formation of a trench as well as element isolation regions and additional semiconductor regions which serve as the source and drain regions of a field effect transistor, although in a somewhat modified form therefrom. Discussion will now turn to the art rejections.

According to the outstanding Office Action, claims 4-7 were rejected under 35 USC §102(b) as anticipated by Baba et al (USP 5,733,810); claims 1-3 were rejected under 35 USC §103 over the combination of Lee (USP 6,200,855) in view of Baba et al (*supra*); and claims 33-35 were rejected under 35 USC §102(b) as anticipated by Kimura et al (USP 5, 177,576). As to the rejection of claim 33, this has been rendered moot in view of the canceling of that claim. However, agreeing to the canceling of that claim should not be construed as an acquiescence with regard to the merits of the rejected thereto. Also, it will be shown, hereinbelow, the invention according to claims 1-3, 4-7 and 34-35 was neither disclosed nor could have been suggested in a manner as that alleged in the outstanding rejections. Therefore, insofar as presently applicable, including with regard to the newly presented claims, these rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

According to independent claim 1, the process (method) calls for, among other aspects thereof, the formation of trenches of which the radius of curvature of the bottom corners is larger than 10 nm in a first semiconductor region of the substrate and, also, calls for the forming of a second semiconductor region as well as a third semiconductor region in the first semiconductor region such that the second and third semiconductor regions have a depth shallower than that of the first semiconductor region and that of the trenches. Also according to claim 1, the second and third semiconductor regions serve as the source and drain regions of the field effect transistor such that the channel forming region thereof is to be formed at the bottom surfaces of the trench and the two side surfaces thereof of the trench between the second and third semiconductor regions. In other words, according to the present invention, the semiconductor regions on the side surfaces

and bottom surface of the trench (e.g., 7) relate to the channel region of the formed field effect transistor with the buried gate electrode structure. An example of this is disclosed, although not limited thereto, with regard to Figs. 31-35 as well as the related discussion in paragraphs [0145] - [0149] in the Substitute Specification. Such is also featured with regard to independent claim 4, as now amended.

Such a scheme as that now called for in claims 1-3 could not have been rendered obvious in a manner as that alleged in the outstanding rejection. Likewise, the invention according to claims 4-7 also could not have been anticipated nor, for that matter, suggested by Baba et al.

Baba et al disclosed a technique for a vertical MOS semiconductor device structure which, applicants submit, is considerably different from that of the present invention. From Baba et al's Fig. 1F structure device, the effective channel region relates to the vertical length of the p-type layer 2 along the side of the trench and, moreover, corner of the bottom portion of the groove 4, it is noted, is formed in the n-type semiconductor substrate 1. Due to this, the roundness of the corner of the bottom portion of the groove 4 does not contribute to a sub-threshold coefficient of a field effect transistor, in clear contradistinction with that effected in accordance with the present invention.

As mentioned above, in accordance with the technique presently called for in claims 1+ and 4+, the side surfaces as well as the underlying surface of the semiconductor region on the bottom of the trench 7 contribute to the channel region of the formed field effect transistor. However, such is clearly not the case according to Baba et al's technique. It is submitted, Baba et al neither disclosed nor suggested the schemed invention according to claims 4+ or, for that matter, according to claims 1-3 when combined, also, with Lee's teachings. That is, Baba

et al neither described nor even hinted at a technique that would have lead to applicants' invention. Therefore, for at least the reasons discussed above, the invention could not have been anticipated nor rendered obvious therefrom, even if Baba et al were to have been combined with Lee in a manner as cited in the outstanding rejection of claims 1-3.

Even if Lee's schemed device would have been modified in the manner as that alleged in the outstanding rejection of claims 1-3, the method is still deficient at least in terms of steps (a) and (d) in claim 1 and, likewise, at least with regard to the steps (a) and (e) according to claim 4. Regarding the control of the radius of curvature in the formation of the trenches, the claims now called for forming the trenches of which the radius of curvature of the bottom corners is larger than 10 nm in the first semiconductor region of the semiconductor substrate. Baba et al's radius of curvature scheme is clearly different from that called for according to the present invention. With regard to the present invention, through employing a step etching scheme such as at the time of forming the trenches, the trenches with large radius of curvature at the bottom corners can be realized while also limiting the undercuts to a small size. This leads to improved characteristics in the formed buried transistor structure, which are extensively discussed in the Specification. Such a scheme as that presently called for could not have been realizable even over the teachings of Baba et al with Lee.

It is noted that with regard to Baba et al's scheme, the n-type layer 7 (in Fig. 1F) has a radius of curvature at the pn junction such as shown in attached **Sketch 1** so that leakage current is increased. This can be seen in connection with the discussion in paragraph [0146] in the Substitute Specification of the present application. Accordingly, Baba et al, it is submitted, clearly, could not give any hint

that would have led one of ordinary skill to achieve the present invention. As disclosed with regard to Figs. 20, 23 of the present Specification, the n-type region (e.g., 15a) is formed in self-alignment with the isolation (e.g., L,2a,2b) and the trench of the gate electrode (e.g., 9) so as to prevent the formation of the radius of curvature at the pn junction. In other words, the depth of the n-type region (e.g., 15a) is uniform within the source/drain forming area such that the entire circumference of the bottom of the n-type region (e.g., 15a) contacts the isolation (e.g., L,2a,2b) of the trench of the gate electrode (e.g., 9).

The technique called for according to claims 34 and 35 also could not have been anticipated nor suggested from Kimura et al's disclosure. In that regard, it is noted that step (g) in the process according to claim 34 has been clarified to remove the concerns raised in the outstanding Office Action. This was discussed earlier in these remarks. According to the process set forth in claim 34, the invention calls for the gate electrode to also be formed inside the first trench. However, the gate electrode 28 in Kimura et al, referred to in the outstanding rejection thereof, is not shown to be inside the trench but rather is an upper horizontal layer outside of the trench along with the gate insulating film thereof. The present invention calls for the second insulating film to be formed over the first insulating film, in clear contradistinction with the referred to insulating film 9 in the outstanding rejections. For these and other reasons, it is clearly apparent that Kimura et al's technique is considerably different from that presently called for.

It is also submitted, the invention according to newly presented claims is patentable for the same and similar reasons as that discussed above. As can be seen from the invention according to claims 51+, a number of the patentably defining featured aspects therein are also included with regard to the previously

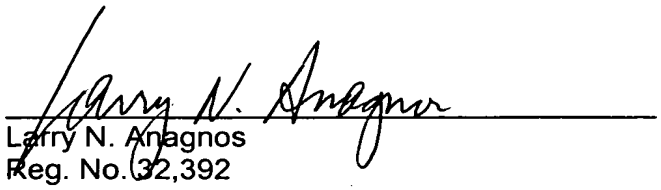
pending claims, as now further amended. Therefore, for the same and similar reasons as that argued above, the newly presented claims 51-56 are also considered patentable.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, reconsideration and withdrawal of the outstanding rejections as well as favorable action on all of the presently pending claims, i.e., claims 1-32, 34-35 and 51-56, and an early formal notification of allowability of the above-identified application is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by a personal interview, the Examiner is invited to contact the undersigned representative at the number indicated below.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (501.39484X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



Larry N. Anagnos
Reg. No. 32,392

LNA/dks
703-312-6600
Attachments: **Sketch 1**

Sketch 1

US005733810A

United States Patent [19]

Baba et al.

[11] Patent Number: 5,733,810

[45] Date of Patent: Mar. 31, 1998

[54] METHOD OF MANUFACTURING MOS TYPE SEMICONDUCTOR DEVICE OF VERTICAL STRUCTURE

[75] Inventors: Yoshiro Baba; Hiroshi Naruse, both of Yokohama, Japan

[73] Assignee: Kabushiki Kaisha Toshiba, Kawasaki, Japan

[21] Appl. No.: 820,530

[22] Filed: Mar. 19, 1997

[30] Foreign Application Priority Data

Mar. 22, 1996 [JP] Japan 8-066495

[51] Int. Cl.[6] H01L 21/70

[52] U.S. Cl. 438/268; 438/270; 438/272

[58] Field of Search 438/268, 270, 438/272, 206, 212

[56] References Cited

U.S. PATENT DOCUMENTS

5,108,938 4/1992 Solomon 438/270

5,349,224 9/1994 Gilbert et al. 438/270

5,532,179 7/1996 Chang et al. 438/270

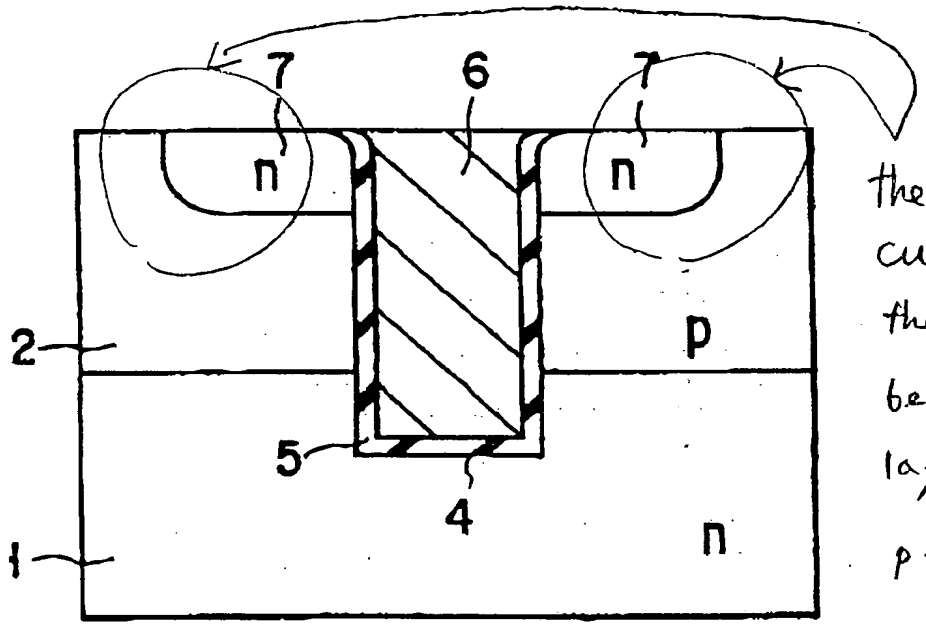
Primary Examiner—Kevin Picardat

Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

[57] ABSTRACT

A groove is formed on a semiconductor substrate. A mask material layer is so formed on the surface of the semiconductor substrate as to open a groove region. With the mask material layer used as a mask, a semiconductor layer is selectively formed on the semiconductor substrate exposed with the inner wall surface of the groove. Then, the mask material layer is removed. An insulating film is formed on the semiconductor layer formed on the inner wall surface of the groove and the surface of the semiconductor substrate. The groove is buried with a conductor.

14 Claims, 4 Drawing Sheets



the radius of curvature of the pn junction between the n-type layer 7 and the p-type layer 2